Half Adder

Let $x$ and $y$ represent bits (0,1). The half adder, which carries out $x + y$ is given by the following table:

| $x$ | $y$ | $s = (x && \neg y) || (\neg x && y)$ | $c = x && y$ |
|-----|-----|-------------------------------------|-------------|
| 1   | 1   | 0                                   | 1           |
| 1   | 0   | 1                                   | 0           |
| 0   | 1   | 1                                   | 0           |
| 0   | 0   | 0                                   | 0           |

The $s$ column represents the sum digit and the $c$ column represents the carry digit. Notice that:

$$s = \begin{cases} 1 & \text{if exactly one of } x \text{ and } y \text{ is 1}, \\ 0 & \text{if } x \text{ and } y \text{ are both 0 or both 1}. \end{cases}$$

In other words,

$$s = (x && \neg y) || (\neg x && y).$$

In addition,

$$c = \begin{cases} 1 & \text{if both } x \text{ and } y \text{ are 1}, \\ 0 & \text{if one or both of } x \text{ and } y \text{ are 0}, \end{cases}$$

or

$$c = x && y.$$

For example,

$$x = 1 \quad y = 1, \quad s = 0, \quad c = 1$$

which corresponds to

```
  1
  1
--
10
```

The electrical circuit for a half adder is shown in Figure 1.

Full Adder

Let $x$, $y$, and $z$ represent bits (0,1). The full adder, which carries out $x + y + z$ where $x$ and $y$ represents bits and $z$ represents the carry bit from adding a previous column of bits. The full adder is given by the following table:
Figure 1: A half adder to add $x + y$. 
The \( s \) column represents the sum digit and the \( c \) column represents the carry digit. Notice that

\[
S = \begin{cases} 
1 & \text{if exactly one of } x, y, \text{ and } z \text{ is 1 or,} \\
0 & \text{if } x, y, \text{ and } z \text{ are 1,} 
\end{cases}
\]

or

\[
S = (x \& \& !y \& \& !z) || (!x \& \& y \& \& !z) || (!x \& \& !y \& \& z) || (x \& \& y \& \& z).
\]

In addition,

\[
C = \begin{cases} 
1 & \text{if exactly two of } x, y, \text{ and } z \text{ are 1 or,} \\
0 & \text{otherwise,} 
\end{cases}
\]

or

\[
C = (x \& \& y \& \& z) || (!x \& \& y \& \& z) || (x \& \& !y \& \& z) || (x \& \& y \& \& !z).
\]

For example,

\[
x = 1, \quad y = 1, \quad z = 1, \quad S = 1, \quad C = 1
\]

which corresponds to

\[
1 \\
1 \\
1 \\
-\-- \\
11
\]

The electrical circuit for a full adder is shown in Figure 2. Although we can construct the circuit from the logical formulae above, it is easier to construct the circuit in terms of half adders and an \textit{or} gate. In the figure \( s_1 \) and \( c_1 \) represent the sum and carry of \( x + y \) and \( s_2 \) and \( c_2 \) represent the sum and carry of \( s_1 + z \). Notice that the final sum \( S \) on the right is the sum obtained from the all three bits \( x, y, \) and \( z \). In addition, the final carry \( C \) on the right is 1 if \( x + y \) has a carry of 1 or \( s_1 + z \) has a carry of 1, or both of these sums have a carry of 1.

For example, suppose that \( x = 1, y = 0, \) and \( z = 1 \). Then

\[
s_1 = 1, \quad c_1 = 0.
\]
Figure 2: A full adder to add $x + y + z$. 
The input to the second half adder is \( z = 1 \) and \( s_1 = 1 \) which gives

\[
s_2 = 0, \quad c_2 = 1.
\]

Therefore,

\[
s = s_2 = 0, \quad c = c_1 | c_2 = 1.
\]

**Two-bit Adder**

A two-bit adder can perform additions such as

\[
\begin{array}{c}
10 \\
11 \\
--- \\
101
\end{array}
\]

In general we would like to sum

\[
\begin{array}{ccc}
a_2 & a_1 \\
b_2 & b_1
\end{array}
\]

\[
\begin{array}{c}
s_3 \\
s_2 \\
s_1
\end{array}
\]

Notice that

- \( s_1 \) is obtained with a half adder applied to \( a_1 \) and \( b_1 \), and let’s suppose this gives a sum bit \( s_1 \) and a carry \( c_1 \).

- \( s_2 \) is obtained with a full adder applied to \( a_1, b_1 \), and the previous carry bit \( c_1 \). Let’s suppose this gives a sum bit \( s_2 \) and a carry \( c_2 \).

- \( s_3 \) is simply the carry bit \( c_2 \).

The electrical circuit for a two-bit adder that corresponds to this scheme is shown in Figure 3.
Figure 3: A two-bit adder.